CLAIMS

We claim:

1. A method of enhancing inductor performance, comprising the steps of:

providing a structure having a first oxide layer formed thereover;

forming a lower low-k dielectric layer over the first oxide layer;

forming a second oxide layer over the lower low-k dielectric layer;

patterning the second oxide layer to form at least one hole there through exposing a portion of the lower low-k dielectric layer;

etching through the exposed portion of the lower low-k dielectric layer and into the lower low-k dielectric layer to from at least one respective air gap within the etched lower low-k dielectric layer;

forming an upper low-k dielectric layer over the patterned second oxide layer; and

forming at least one inductor within the upper low-k dielectric layer and over the at least one air gap whereby the performance of the at least one inductor is enhanced.

2. The method of claim 1, wherein the structure is silicon, germanium, gallium arsenide, any compounded semiconductor or a polymeric material.

3. The method of claim 1, wherein the structure is comprised of silicon.

4. The method of claim 1, wherein the structure includes one or more levels of metal interconnects with an uppermost exposed metal interconnect.

5. The method of claim 1, wherein the first oxide layer has a thickness of from about 1000 Å to 5μm; the lower low-k layer has a thickness of from about 1000 to 10,000Å and the second oxide layer has a thickness of from about 1000 to 10,000Å.

6. The method of claim 1, wherein the first oxide layer has a thickness of from about 3000 to 6000Å; the lower low-k layer has a thickness of from about 2000 to 6000Å and the second oxide layer has a thickness of from about 4000 to 8000Å.

7. The method of claim 1, wherein the upper low-k dielectric layer has a thickness of from about 0.1 to 10.0μm.

8. The method of claim 1, wherein the upper low-k dielectric layer has a thickness of from about 2.0. to 5.0μm.

9. The method of claim 1, wherein the first oxide layer is comprised of silicon oxide, doped silicon oxide, BPSG, FSG, silicon carbide (SiC), Coral™, Black Diamond™, SiN or TEOS; the lower low-k dielectric layer is comprised of silicon oxide, boron-doped silicon oxide, phosphorous-doped silicon oxide, BPSG, FSG, SiN or carbon doped silicon oxide such as Coral™ or Black Diamond™ and the upper oxide layer is comprised of silicon oxide, doped silicon oxide, BPSG, FSG, Coral™, Black Diamond™, SiN or silicon carbide (SiC).

10. The method of claim 1, wherein the first oxide layer is comprised of silicon oxide; the lower low-k dielectric layer is comprised of carbon-doped silicon oxide and the upper oxide layer is comprised of silicon oxide.

11. The method of claim 1, wherein the upper low-k dielectric layer is comprised of silicon oxide, TEOS, SiC, SiN, FSG, BPSG, carbon-doped silicon oxide, Coral™ or Black Diamond™.

12. The method of claim 1, wherein the upper low-k dielectric layer is comprised of FSG.

13. The method of claim 1, including the step of forming a dual damascene structure within the first oxide layer and the lower low-k dielectric layer proximate the at least one air gap before formation of the at least one air gap.

14. The method of claim 1, wherein two or more air gaps are formed.

15. The method of claim 1, wherein two or more inductors are formed over the air gap.

16. The method of claim 1, wherein two or more air gaps are formed and two or more inductors are formed over the two or more air gaps.

17. The method of claim 1, wherein the at least one hole has a diameter of from about 1.0 to 10.0μm and the at least one air gap has a diameter of from about 100.0 to 500.0μm.

18. The method of claim 1, wherein the hole has a diameter of from about 2.0 to 6.0μm and the air gap has a diameter of from about 200.0 to 400.0μm.

19. The method of claim 1, wherein the lower low-k dielectric layer is etched using an etch selected from the group consisting of: a dry etch, a wet etch and a combination wet and dry etch.

20. The method of claim 1, wherein the lower low-k dielectric layer is etched using a dry etch.

21. The method of claim 1, wherein the lower low-k dielectric layer is etched using an etch having an oxide : lower low-k dielectric selectivity of about 1:10.

22. The method of claim 1, wherein the lower low-k dielectric layer 14 is etched using an etch having an oxide : lower low-k dielectric selectivity of from about 1:50 to 1:100 .

23. The method of claim 1, wherein the performance of the inductor is enhanced by lowering the capacitance loss of the inductor.

24. The method of claim 1, wherein the performance of the inductor is enhanced by lowering the substrate loss due to eddy currents.

25. The method of claim 1, wherein the performance of the inductor is enhanced by lowering the capacitance loss of the inductor and by lowering the substrate loss due to eddy currents.

26. A method of enhancing inductor performance, comprising the steps of:

providing a structure having a first oxide layer formed thereover to a thickness of from about 1000 Å to 5μm;

forming a lower low-k dielectric layer over the first oxide layer to a thickness of from about 1000 to 10,000Å;

forming a second oxide layer over the lower low-k dielectric layer to a thickness of from about 1000 to 10,000Å;

patterning the second oxide layer to form one or more holes there through exposing one or more respective portions of the lower low-k dielectric layer;

etching through the one or more exposed portions of the lower low-k dielectric layer and into the lower low-k dielectric layer to from one or more respective air gaps within the etched lower low-k dielectric layer;

forming an upper low-k dielectric layer over the patterned second oxide layer; and

forming one or more inductors within the upper low-k dielectric layer and over the one or more air gaps whereby the performance of the one or more inductors is enhanced.

27. The method of claim 26, wherein the structure is comprised of silicon, germanium, gallium arsenide, any compounded semiconductor or a polymeric material.

28. The method of claim 26, wherein the structure is comprised of silicon.

29. The method of claim 26, wherein the structure includes one or more levels of metal interconnects with an uppermost exposed metal interconnect.

30. The method of claim 26, wherein the first oxide layer has a thickness of from about 3000 to 6000Å; the lower low-k layer has a thickness of from about 2000 to 6000Å and the second oxide layer has a thickness of from about 4000 to 8000Å.

31. The method of claim 26, wherein the upper low-k dielectric layer has a thickness of from about 0.1 to 10.0μm.

32. The method of claim 26, wherein the upper low-k dielectric layer has a thickness of from about 2.0. to 5.0μm.

33. The method of claim 26, wherein the first oxide layer is comprised of silicon oxide, doped silicon oxide, BPSG, FSG, silicon carbide (SiC), Coral™, Black Diamond™, SiN or TEOS; the lower low-k dielectric layer is comprised of silicon oxide, boron-doped silicon oxide, phosphorous-doped silicon oxide, BPSG, FSG, SiN or carbon doped silicon oxide such as Coral™ or Black Diamond™ and the upper oxide layer is comprised of silicon oxide, doped silicon oxide, BPSG, FSG, Coral™, Black Diamond™, SiN or silicon carbide (SiC).

34. The method of claim 26, wherein the first oxide layer is comprised of silicon oxide; the lower low-k dielectric layer is comprised of carbon-doped silicon oxide and the upper oxide layer is comprised of silicon oxide.

35. The method of claim 26, wherein the upper low-k dielectric layer is comprised of silicon oxide, TEOS, SiC, SiN, FSG, BPSG, carbon-doped silicon oxide, Coral™ or Black Diamond™.

36. The method of claim 26, wherein the upper low-k dielectric layer is comprised of FSG.

37. The method of claim 26, including the step of forming a dual damascene structure within the first oxide layer and the lower low-k dielectric layer proximate the one or more air gaps before formation of the one or more air gaps.

38. The method of claim 26, wherein the one or more holes have respective diameters of from about 1.0 to 10.0μm and the one or more air gaps have respective diameters of from about 100.0 to 500.0μm.

39. The method of claim 26, wherein the one or more holes have respective diameters of from about 2.0 to 6.0μm and the one or more air gaps have respective diameters of from about 200.0 to 400.0μm.

40. The method of claim 26, wherein the lower low-k dielectric layer is etched using an etch selected from the group consisting of: a dry etch, a wet etch and a combination dry and wet etch.

41. The method of claim 26, wherein the lower low-k dielectric layer is etched using a dry etch.

42. The method of claim 26, wherein the lower low-k dielectric layer is etched using an etch having an oxide : lower low-k dielectric selectivity of about 1:10.

43. The method of claim 26, wherein the lower low-k dielectric layer is etched using an etch having an oxide : lower low-k dielectric selectivity of from about 1:50 to 1:100.

44. The method of claim 26, wherein the performance of the one or more inductors is enhanced by lowering the capacitance loss of the one or more inductors.

45. The method of claim 26, wherein the performance of the one or more inductors is enhanced by lowering the substrate loss due to eddy currents.

46. A method of enhancing inductor performance, comprising the steps of:

providing a structure having a first oxide layer formed thereover;

forming a lower low-k dielectric layer over the first oxide layer;

forming a second oxide layer over the lower low-k dielectric layer;

patterning the second oxide layer to form one or more holes there through exposing one or more respective portions of the lower low-k dielectric layer;

etching through the one or more exposed portions of the lower low-k dielectric layer and into the lower low-k dielectric layer to from one or more respective air gaps within the etched lower low-k dielectric layer; the one or more air gaps having respective diameters of from about 100.0 to 500.0μm;

forming an upper low-k dielectric layer over the patterned second oxide layer; and

forming one or more inductors within the upper low-k dielectric layer and over the one or more air gaps whereby the performance of the one or more inductors is enhanced.

47. The method of claim 46, wherein the first oxide layer has a thickness of from about 1000 Å to 5μm; the lower low-k layer has a thickness of from about 1000 to 10,000Å and the second oxide layer has a thickness of from about 1000 to 10,000Å.

48. The method of claim 46, wherein the first oxide layer has a thickness of from about 3000 to 6000Å; the lower low-k layer has a thickness of from about 2000 to 6000Å and the second oxide layer has a thickness of from about 4000 to 8000Å.

49. The method of claim 46, wherein the upper low-k dielectric layer has a thickness of from about 0.1 to 10.0μm.

50. The method of claim 46, wherein the upper low-k dielectric layer has a thickness of from about 2.0. to 5.0μm.

51. The method of claim 46, wherein the first oxide layer is comprised of silicon oxide, doped silicon oxide, BPSG, FSG, silicon carbide (SiC), Coral™, Black Diamond™, SiN or TEOS; the lower low-k dielectric layer is comprised of silicon oxide, boron-doped silicon oxide, phosphorous-doped silicon oxide, BPSG, FSG, SiN or carbon doped silicon oxide such as Coral™ or Black Diamond™ and the upper oxide layer is comprised of silicon oxide, doped silicon oxide, BPSG, FSG, Coral™, Black Diamond™, SiN or silicon carbide (SiC).

52. The method of claim 46, wherein the first oxide layer is comprised of silicon oxide; the lower low-k dielectric layer is comprised of carbon-doped silicon oxide and the upper oxide layer is comprised of silicon oxide.

53. The method of claim 46, wherein the upper low-k dielectric layer is comprised of silicon oxide, TEOS, SiC, SiN, FSG, BPSG, carbon-doped silicon oxide, Coral™ or Black Diamond™.

54. The method of claim 46, wherein the upper low-k dielectric layer is comprised of FSG.

55. The method of claim 46, including the step of forming a dual damascene structure within the first oxide layer and the lower low-k dielectric layer proximate the one or more air gaps before formation of the one or more air gaps.

56. The method of claim 46, wherein the one or more holes have respective diameters of from about 1.0 to 10.0μm.

57. The method of claim 46, wherein the one or more holes have respective diameters of from about 2.0 to 6.0μm and the one or more air gaps have respective diameters of from about 200.0 to 400.0μm.

58. The method of claim 46, wherein the lower low-k dielectric layer is etched using an etch selected from the group consisting of: a dry etch, a wet etch and a combination wet and dry etch.

59. The method of claim 46, wherein the lower low-k dielectric layer is etched using a dry etch.

60. The method of claim 46, wherein the lower low-k dielectric layer is etched using an etch having an oxide : lower low-k dielectric selectivity of about 1:10.

61. The method of claim 46, wherein the lower low-k dielectric layer is etched using an etch having an oxide : lower low-k dielectric selectivity of from about 1:50 to 1:100.

62. The method of claim 46, wherein the performance of the one or more inductors is enhanced by lowering the capacitance loss of the one or more inductors.

63. The method of claim 46, wherein the performance of the one or more inductors is enhanced by lowering the substrate loss due to eddy currents.